9119	37145	JJJJJJJJ	L timer 1 control,
911A	37146	KKKKKKKK	M timer 2 control
911B	37147	LLMNNNOP	N shift register control
911C	37148	QQQRSSST	O port B latch enable
911D	37149	UVWXYZab	P port A latch enable
911E	37150	cdefghij	Q CB2 control
911F	37151	kkkkkkkk	R CB1 control
			S CA2 control
			T CA1 control
			U IRQ status
			V timer 1 time-out
			W timer 2 time-out
			X CB1 pin active transition
			Y CB2 pin active transition
			Z completion of 8 shifts
			a CA1 pin active transition
			b CA2 pin active transition
			c enable control
			d timer 1 time-out enable
			e timer 2 time-out enable
			f CB1 interrupt enable
			g CB2 interrupt enable
			h shift interrupt enable
			i CA1 interrupt enable
			j CA2 interrupt enable
			k port A (no handshaking)
9110	37136	VIA1PB	Port B input / output register
		→	bit 7 Data Set Ready (DSR) IN X-line
		→	bit 6 Clear to Send (CTS) IN X-line
			bit 5 unused
		→	bit 4 Data Carrier Detect (DCD) IN X-line
		→	bit 3 Ring Indicator (RI) IN
		←	bit 2 Data Terminal Ready (DTR) OUT X-line
		←	bit 1 Request To Send (RTS) OUT X-line
		→	bit 0 Received Data Signal (Sin) IN X-line, 3 line
9111	37137	VIA1PA1	Port A input / output register
		←	bit 7 serial attention out
		→	bit 6 tape button down flag (cassette switch)
		→	bit 5 light pen / joystick FIRE
		→	bit 4 joystick LEFT off (JOY 2)
		→	bit 3 joystick DOWN off (JOY 1)
		→	bit 2 joystick UP off (JOY 0)
		→	bit 1 serial data IN
		→	bit 0 serial clock IN
9112	37138	VIA1DDRB	Data direction register B (also see bit 1 of 37147)
			1 in bit indicates OUTPUT in port B (37136)

9113	37139	VIAIDDRA	Data direction register A (also see bit 0 of 37147)
			1 in bit indicates OUTPUT in port A (37137)
9114	37140	VIA1T1CL	Timer 1 low byte (LSB)
9115	37141	VIA1TICH	Timer 1 high byte & counter (MSB)
			setting this byte for timer 1 starts timer
9116	37142	VIA1T1LL	Timer 1 low byte (LSB)
9117	37143	VIA1T1LH	Timer 1 high byte (MSB)
9118	37144	VIA1T2CL	Timer 2 low byte (LSB)
9119	37145	VIA1T2CH	Timer 2 high byte (MSB)
911A	37146	VIA1SR	Shift register for parallel and serial conversion
			NOTE: the KERNAL does not use this shift register
			bit 7 shift out onto CB2 line
			bit 4-2 aux control register at 37147 select shift reg
			bit 2 interrupt enable and interrupt flag corresponds
911B	37147	VIA1ACR	Auxiliary control register
			A bit 7-6 timer 1 options: PB7 output (neg, square)
		AABCCCDE	00 single interval more, no PB7 output pulse
			01 free run more, no PB7 output pulse
			10 single interval more, PB7 negative pulsed
			11 single interval more, PB7 negative pulsed
			B bit 5 timer 2 options
			0 single interval timing
			1 countdown incoming PB6 pulses
			C bit 4-2 shift register options
			000 shift register disabled
			001 input CB2 shift bit 0, timer 2, output clock CB1
			010 input CB2 shift bit 0, system, output clock CB1
			011 output CB2 bit 7, timer 2, output clock CB1
			100 output CB2 bit 7, timer 2 as delay clock
			110 output CB2 bit 7, system, output clock CB1
			111 output CB2 bit 7, output external clock, in CB1
			D bit 1 Port B (location 37136 $9110)
			0 port B reflects changing values on pins
			1 port in latch mode (input CB1 interrupt occurred)
			E bit 0 Port A (location 37137 $9111)
			0 port A reflects changing values on pins
			1 port in latch mode (input CA1 interrupt occurred)
911C	37148	VIA1PCR	Peripheral control register (handshake)
			A bit 7 CB2 line control input output mode
		ABBCDDDE	0 input mode
			1 output mode
			B bit 6-5 CB2 line control
			00 IFR bit 3 high to low CB2, clears IFR
			01 IFR bit 3 high to low CB2, does not clear IFR
			10 IFR bit 3 low to high CB2, clears IFR
			11 IFR bit 3 low to high CB2, does not clear IFR

			C bit 4 CB1 line control low (0) or high (1)
			0 IFR bit 4 high to low transition of CB1 (default)
			1 IFR bit 4 low to high transition of CB1
			D bit 3-1 CA2 line control
			000 IFR bit 0 high to low CA2, clears CA2
			001 IFR bit 0 high to low CA2, does not clear CA2
			010 IFR bit 0 low to high CA2, clears CA2
			011 IFR bit 0 low to high CA2, does not clear CA2
			100 output (handshake) CA2 low
			101 output mode (pulse)
			110 output mode (manual), CA2 low
			111 output mode (manual), CA2 high
			E bit 0 CA1 line control low (0) or high (1)
			0 IFR bit 4 high to low transition of CA1
			1 IFR bit 4 low to high transition of CA1
911D	37149	VIA11FR	Interrupt flag register (IFR) (service order 1,6,5,4)
			bit 7 IRQ status (NMI)
	NMI Interrupts	←	bit 6 timer 1 interrupt flag, RS-232 send
	service order	→	bit 5 timer 2 interrupt flag, RS-232 receive
	bit 1	→	bit 4 CB1 interrupt flag, RS-232 receive
	bit 6		bit 3 CB2 interrupt flag
	bit 5		bit 2 shift register flag
	bit 4	→	bit 1 CA1 interrupt flag
	*not by kernal routine	←	bit 0 CA2 interrupt flag, tape motor, if STOP, BRK
911E	37150	VIA11ER	Interrupt enable register (IER)
			bit 7 IER set / clear control (1 enable IFR)
			bit 6 timer 1 interrupt enable
			bit 5 timer 2 interrupt enable
			bit 4 CB1 interrupt enable
			bit 3 CB2 interrupt enable
			bit 2 shift register enable
			bit 1 CA1 interrupt enable
			bit 0 CA2 interrupt enable
911F	37151-37167		6522 Versatile Interface Adapter 2
911F	37151	VIA1PA2	Port A (sense tape switch); mirror of 37137
9120	37152	VIA2PB	Port B input / output register; Key column scan
			default value 247 except when SCNKEY or UDTIM
		↔	bit 7 (127) key column 7; Joy 3, pin 4 game port
		←	bit 6 (191) key column 6
		←	bit 5 (223) key column 5
		←	bit 4 (239) key column 4
		←	bit 3 (247) key column 3; tape write, port E-5
		←	bit 2 (251) key column 2
		←	bit 1 (253) key column 1
		←	bit 0 (254) key column 0
NAIL			see value chart in 37153

9121	37153	VIA2PA1	Port A input / output register; Keyboard row scan bit 7-0 keyboard row 7-0, respectively

	7	6	5	4	3	2	1	0
← 7	F7	F5	F3	F1	↕	⇔	Rt	De
← 6	HO	↑	=	Ri	/	;	*	£
← 5	-	@	:	.	,	L	P	+
← 4	0	O	K	M	N	J	I	9
← 3	8	U	H	B	V	G	Y	7
← 2	6	T	F	C	X	D	R	5
← 1	4	E	S	Z	Lf	A	W	3
← 0	2	Q	C=	SPC	St	Ct	←	1

column stored in 37152 ($9120)

9122	37154	VIA2DDRB	Data direction register B when a bit is set to 0, port B but is used for input 127 set direction for controller, some keys ignored 255 all lines as output (default and restore value)
9123	37155	VIA2DDRA	Data direction register A when a bit is set to 0, port A but is used for input 0 (default and restore value) Power-on/reset, RUN/STOP-RESTORE sets to 0
9124	37156	VIA2T1CL	Timer 1, low byte latch (LSB) used to generate the IRQ 60 times per second
9125	37157	VIA2T1CH	Timer 1, high byte latch (MSB) setting this byte of timer to 1 starts timer running
9126	37158	VIA2T1LL	Timer 1, low byte counter (LSB)
9127	37159	VIA2T1HL	Timer 1, high byte counter (MSB)
9128	37160	VIA2T2CL	Timer 2, low byte latch (LSB) timer used by the KERNAL for detecting timeouts
9129	37161	VIA2T2CH	Timer 2, high byte latch (MSB)
912A	37162	VIA2SR	Shift register for parallel and serial conversion
912B	37163	VIA2ACR	Auxiliary control register A bit 7-6 timer 1 options (single/free, PB7)
		AABCCCDE	B bit 5 timer 2 (0 single interval, 1 count PB6 pulse) C bit 4-2 shift register options 000 shift disabled 001 input on CB2 using timer 2 010 input on CB2 using system clock 011 output on CBs using timer 2 100 output on CB2 using timer 2 delay 110 output on CB2 using system clock 111 output on CB2 using external clock D bit 1 Port B latch enable options E bit 0 Port A latch enable options
912C	37164	VIA2PCR	Peripheral control register (handshake) A bit 7-5 CB2 line control, data out
		AAABCCCD	000 input mode IFR bit 3 hi and clear CB2

			001 input mode IFR bit 3 hi and do not clear 010 input mode IFR bit 3 lo and clear CB2 011 input mode IFR bit 3 lo and do not clear 100 output mode (handshake) CB2 low 110 output mode (pulse) CB2 low 111 output mode (manual) CB2 high 000 shift disabled
			B bit 4 CB1 SRQ IN (0 high to low, 1 low to high)
			C bit 3-1 CA2 line control, serial clock out 000 input mode IFR bit 0 hi and clear CA2 001 input mode IFR bit 3 hi and do not clear 010 input mode IFR bit 3 lo and clear CA2 011 input mode IFR bit 3 lo and do not clear 100 output mode (handshake) CA2 low 110 output mode (pulse) CA2 low 111 output mode (manual) CA2 high 000 shift disabled
			D bit 0 CA1 line control, TAPE read line
912D	37165 *not by kernal routine	VIA2IFR	Interrupt flag register (IFR) bit 7 IRQ occurred (0 clears all interrupts) bit 6 timer 1 interrupt, Normal IRQ handler (1/60s) bit 5 timer 2 interrupt, Tape IRQ handler, Tape write bit 4 CB1 transition interrupt * bit 3 CB2 transition interrupt * bit 2 shift register interrupt * bit 1 CA1 transition interrupt, Tape IRQ, Tape read bit 0 CA2 transition interrupt
912E	37166	VIA2IER	Interrupt enable register (IER) bit 7 IFR enable (1) disable (1) bit 6 timer 1 interrupt enable (1) bit 5 timer 2 interrupt bit 4 CB1 interrupt bit 3 CB2 interrupt bit 2 shift register interrupt bit 1 CA1 (TAPE I/O) interrupt bit 0 CA2 interrupt
912F	37167	VIA2PA2	Port A output register; mirror 37153
9130	37168-		Unused I/O for future expansion block1
9400	37888-38399	COLORMA AAAABCCC	Color RAM map for 8k+ expansion A bit 7-4 not used B bit 3 multicolor enable (1) disable default (0) C bit 2-0 foreground color (default value 1)
9600	38400-38911	COLORMA	Color RAM map for unexp. and +3K expansion bit 7-4 not used bit 3 multicolor enable (1) disable default (0) bit 2-0 foreground color (default value 1)